Amendments to Claims:

1. (Currently Amended) A method including:

in a queue, writing a first microinstruction of a plurality of microinstructions to a first location indicated by a write pointer, the plurality of microinstructions being written to the queue as a set of a predetermined number of microinstructions, and the first microinstruction of the plurality of microinstructions being indicated as invalid on account of being outside a ~~macroinstruction~~ trace of microinstructions, wherein the trace of microinstructions comprises a head entry, the head entry comprising a linear address to determine a set of subsequent entries in the trace;

making a qualitative determination whether or not to retain the first microinstruction within the queue based on the indicated invalidity of the first microinstruction[[s]];

if the qualitative determination is to retain the first microinstruction, then advancing the write pointer to indicate a second location within the queue into which to write a second microinstruction; and

if the qualitative determination is not to retain the first microinstruction, then maintaining the write pointer to indicate the first location within the queue into which to write the second microinstruction, so that the first microinstruction is overwritten by the second microinstruction.

2. (Previously Presented) The method of claim 1 wherein the qualitative determination includes examining a valid bit associated with the first microinstruction to determine validity of the first microinstruction, making the qualitative determination to retain the first microinstruction if the valid bit indicates the first microinstruction is being valid, and making the qualitative determination not to retain the first microinstruction if the valid bit indicates the first microinstruction as being invalid.

3. (Canceled)

4. (Previously Presented) The method of claim 2 wherein a plurality of microinstructions are written to the queue in a set of a predetermined number of microinstructions, and wherein at

least one microinstruction of the set is indicated as being invalid on account of a branch misprediction relating to a branch microinstruction upstream of the at least one microinstruction in a stream of microinstructions.

5. (Canceled)

6. (Previously Presented) The method of claim 1 wherein the first microinstruction is written to the queue from a microinstruction cache.

7. (Previously Presented) The method of claim 6 wherein the first microinstruction is part of a trace of microinstructions received from the microinstruction cache.

8. (Currently Amended) The method of claim 6 wherein the first microinstruction is received from [[an]] a microinstruction source operating in a first clocking domain into the queue and read from the queue to an microinstruction destination operating in a second clocking domain.

9. (Currently Amended) The method of claim 1 wherein the first microinstruction is received into the queue as part of a set of microinstructions comprising a first predetermined number of microinstructions and read from the queue to [[an]] a microinstruction destination as part of a second set of microinstructions comprising a second number of microinstructions.

10. (Previously Presented) The method of claim 1 wherein the first microinstruction is written from a source to a destination, and wherein the queue comprises a first path between source and destination, the method including propagating the first microinstruction from the source to the destination via a second path, not including the queue, if the queue is empty.

11. (Previously Presented) The method of claim 10 including selecting between the first and second paths to receive the first microinstruction for propagation to the destination.

12. (Previously Presented) The method of claim 1 wherein the queue includes a first portion

to support a first thread within a multithreaded environment and a second portion to support a second thread within the multithreaded environment, and wherein the first location into which the first microinstruction is written is located in the first portion if the first microinstruction comprises part of the first thread.

13. (Currently Amended) Apparatus comprising:

a queue to buffer a first microinstruction propagated from a source to a destination; and

write logic to make a qualitative determination whether or not to retain the first microinstruction within the queue; if the qualitative determination is to retain the first microinstruction, to advance a write pointer to indicate a second location within the queue into which to write a second microinstruction; and, if the qualitative determination is not to retain the first microinstruction, to maintain the write pointer to indicate the first location within the queue into which to write the second microinstruction, so that the first microinstruction is overwritten by the second microinstruction[[.]];

wherein the first microinstruction is written to the queue as part of a set including a predetermined number of microinstructions, and wherein at least one microinstruction of the set is indicated as being invalid on account of being outside a ~~macroinstruction~~ trace of microinstructions, wherein the trace of microinstructions comprises a head entry, the head entry comprising a linear address to determine a set of subsequent entries in the trace.

14. (Previously Presented) The apparatus of claim 13 wherein the write logic is to examine a valid bit associated with the first microinstruction to determine validity of the first microinstruction, to make the qualitative determination to retain the first microinstruction if the valid bit indicates the first microinstruction as being valid, and to make the qualitative determination not to retain the first microinstruction if the valid bit indicates the first bit as being invalid.

15. (Canceled)

16. (Previously Presented) The apparatus of claim 14 wherein the first microinstruction is written to the queue as part of a set of a predetermined number of microinstructions, and wherein

at least one microinstruction of the set is indicated as being invalid on account of a branch misprediction relating to a branch microinstruction upstream of the at least one microinstruction in a stream of microinstructions.

17. (Canceled)

18. (Currently Amended) The apparatus of claim ~~1~~ 13 wherein the source from which the first microinstruction is written to the queue comprises a microinstruction cache.

19. (Canceled)

20. (Previously Presented) The apparatus of claim 13 wherein the queue comprises a first path between the source and the destination, the apparatus including a second path between the source and destination, not including the queue, and wherein the write logic directs the first microinstruction to be propagated between the source and destination via the second path if the queue is empty.

21. (Currently Amended) A machine-readable medium storing a sequence of microinstructions that, when executed by a machine, cause the machine to perform the steps of:

in a queue, writing a first microinstruction of a plurality of microinstructions to a first location indicated by a write pointer, the plurality of microinstructions being written to the queue as a set of a predetermined number of microinstructions, and the first microinstruction of the plurality of microinstructions being indicated as invalid on account of being outside a ~~macroinstruction~~ trace of microinstructions, wherein the trace of microinstructions comprises a head entry, the head entry comprising a linear address to determine a set of subsequent entries in the trace;

making a qualitative determination whether or not to retain the first microinstruction within the queue based on the indicated invalidity of the first microinstruction[[s]];

if the qualitative determination is to retain the first microinstruction, then advancing the write pointer to indicate a second location within the queue into which to write a second microinstruction; and

if the qualitative determination is not to retain the first microinstruction, then maintaining the write pointer to indicate the first location within the queue into which to write the second microinstruction, so that the first microinstruction is overwritten by the second microinstruction.

22. (Currently Amended) The machine-readable medium of claim 21 wherein the sequence of microinstructions cause a multiprocessor to perform the step of examining a valid bit associated with the first microinstruction to determine validity of the first microinstruction, to make the qualitative determination to retain the first microinstruction if the valid bit indicates the first microinstruction as being valid, and to make the qualitative determination not to retain the first microinstruction if the valid bit indicates the first microinstruction as being invalid.